performing process 80 is shown. The data buffers, 18a-18n, and cell numbers of FIG. 2C correspond to the same numbers shown in Figs. 1 and 2B. As shown in FIG. 2C, a system performing process 80 causes the two cells of data buffer 18a to be transmitted before the transmission of the first cell of data buffer 18b is begun. Likewise, data buffer 18b completes transmission before the first cell of data buffer 18c begins transmission, and so forth. --

A2 cont.

In the claims:

Add claims 25 through 31.

-- 25. (New) A processing system for managing queue entries comprising:

a processor;

a memory to store queue entries; and

a storage-medium accessible by the processor to store executable instructions, which when accessed by the processor causes the processor to:

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store addresses in a first queue entry as a linked list, each of the stored addresses including a cell count;

retrieve a first address from the first queue entry; and

modify the linked list of addresses of the first queue entry based on the cell count of the first address retrieved.

26. (New) The system of claim 1, wherein modifying comprises:

decrementing the cell count of the first address each time the first address is retrieved.

27. (New) The method of claim 26, further comprising instructions, which when accessed by the processor causes the processor to:

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determine the cell count is zero; and

set a second address as the first address of the first queue entry.

28. (New) The system of claim 27, wherein storing addresses further comprises:

setting the first address as the head address of the first queue entry; and

linking a second address to the first address of the first queue entry.

29. (New) The system of claim 28, wherein linking the second address to the first address further comprises instructions, which when accessed by the processor causes the processor to:

setting the second address as a tail address of the first queue entry.

30. (New) The system of claim 29, further comprises instructions, which when accessed by the processor causes the processor to:

link a third address to the first queue entry by storing the third address in the location indicated by the tail address.

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31. (New) The system of claim 29, further comprises instructions, which when accessed by the processor causes the processor to:

increment a queue count each time an address is linked to the first queue entry. --

In the drawings:

Enclosed is one amended page of drawings for the application with changes indicated in red.